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PATENT APPLICATION

PASSIVATION SCHEME FOR BUMPED WAFERS

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PASSIVATION SCHEME FOR BUMPED WAFERS

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates to bumped wafers for chip devices, and more particularly, to a new passivation scheme for bumped wafers.

2. Description Of The Prior Art

The primary component of today's chip devices is at least one die. The die generally consists of a wafer that has been passivated. The passivation process for today's wafers generally include masking steps and an expensive planarization process.

Because of the masking layers, the metal layer(s) is generally thinner. In a MOSFET device, a passivation layer is placed over the metal layer to protect it. This can result in an increased resistance from the drain to the source region when the chip device is on. Conventional passivation methods include using silicon nitride as a passivation layer. However, as noted, such use can result in extra steps and increased processing expanse in wafer manufacture.

SUMMARY OF THE INVENTION

The present invention provides a bumped wafer that includes two titanium layers sputtered alternatingly with two copper layers over a non-passivated die. Presently, the bumped wafer includes under bump material under the solder bumps contained thereon.

The present invention also provides a method of making the bumped wafer. The method includes providing a non-passivated die and alternatingly sputtering titanium, copper and titanium and copper thereon. A photo process is then performed and an isolation etch is performed in order to remove the top copper layer, the second titanium layer and the bottom copper layer at the isolation location. A photo process is then once again performed in order to create an area for the under bump material that is under the solder bumps. The top layers of copper and titanium are then etched away at the locations on the wafer where the solder bumps will be placed. The under bump material

is then deposited thereon and the solder is placed over the under bump material. The photo resist material is then stripped away and the bottom layer of titanium is etched at the isolation locations. The remaining top layer of the copper is then etched away and the solder is reflowed in order to shape the solder into a substantially "ball" shape.

Thus, the present invention provides a bumped wafer and a method of manufacture thereof wherein the bumped wafer includes a titanium passivation layer. The titanium tends to passive itself and adhere well to copper as well as aluminum thereby forming a good interlayer. Solder does not wet to the titanium layer, thus providing for defined solderable surfaces in a wafer. Additionally, the copper interlayers (over the aluminum) offer a solderable surface that can be plated and/or sputtered.

Other features and advantages of the present invention will be understood upon reading and understanding the detailed description of the preferred exemplary embodiments, found hereinbelow in conjunction with reference to the drawings in which like numerals represent like elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1K illustrate a bumped wafer in various stages of manufacture in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

Figure 1K schematically illustrates a bumped wafer 10 in accordance with the present invention. The bumped wafer includes a non-passivated die and various layers of material deposited thereon. Additionally, the bumped wafer includes solder bumps.

Turning to Figure 1A, a non-passivated die 11 is illustrated. Figure 1B illustrates the non-passivated die with a first layer of titanium 12 sputtered thereon, a first layer of copper 13 sputtered on the first layer of titanium, a second layer of titanium 14 sputtered on the first layer of copper, and a second layer of copper 15 sputtered on the second layer of titanium.

Turning to Figure 1C, a photo resist material 20 is placed over the second layer of copper for isolation purposes. Figure 1D illustrates the etching away of the photo resist layer along with the second layer of copper, the second layer of titanium and the first layer of copper between region A and region B that are to be isolated. Photo resist material 21 is then placed on the die in such a manner that region C and region D are

exposed as can be seen in Figure 1E. As illustrated in Figure 1F, the second layers of copper and titanium are then etched from regions C and D.

Turning to Figure 1G, solder 22 is plated in regions C and D with an amount of copper as layer 23. A photoresist layer 24 is provided and solder bumps 25 are placed over solder 22.

As can be seen in Figure 1H, the photo resist is then stripped away from regions A and B. The first layer of titanium is then etched out of the isolation area as can be seen in Figure 1I. As can be seen in Figure 1J, the second layer of copper is then etched from the regions A and B and the solder is reflowed so that the solder takes on a substantially "ball" shape as can be seen in Figure 1K.

Thus, the present invention provides a bumped wafer for use in a chip device. For example, the bumped wafer may be formed to provide MOSFETs in the chip device. The copper interlayers are over the aluminum of the non-passivated die and offer a solderable surface that can be plated or sputtered. The copper has a higher conductivity (thermal and electrical) when compared to aluminum and additionally, thicker copper layers are easier to fabricate in comparison to thicker aluminum layers. Use of the titanium as a passivation layer eliminates the need for using silicon nitride or other conventional passivation methods. The titanium tends to passivate itself and adheres well to copper as well as aluminum forming a good interlayer. The thick copper layer on the aluminum layer reduces R_{ds}-on.

Those skilled in the art will understand that the wafer may be manufactured without solder bumps. The solder bumps would then be added later during the manufacturing process of the chip device.

Although the invention has been described with reference to specific exemplary embodiments, it will appreciated that it is intended to cover all modifications and equivalents within the scope of the appended claims.